(54) [TITLE OF THE INVENTION]

Ceramic wiring substrate and ceramic wiring substrate-mounted structure

(57) [ABSTRACT] (Amended)

[Object] To enable the formation of a solder connection electrode having high reliability on the back surface of a thick film multilayer ceramic substrate.

[Construction] A ceramic wiring substrate comprising solder connection electrode 18 and input/output signal pin 3, wherein solder connection electrode 18 is formed on the back surface side of ceramic wiring substrate 1 to which input/output signal pin 3 is connected, and comprises: stress relaxation layer 4, connected directly to wiring conductor 7, comprising a metal layer in a circular form adhering to the back surface of the ceramic; insulating layer 6; connection metal layer 2 in a circular form adhering to the surface of the stress relaxation layer through connection through hole opening 9 formed in the insulating layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and cover coat layer 5 covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material, wherein the stress applied

to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening, wherein the input/output signal pin is directly connected by soldering to the connection metal layer.

[CLAIMS]

[Claim 1] A ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate,

the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[Claim 2] A ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate,

the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being

comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter smaller than the root outer diameter of the input/output signal pin, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[Claim 3] A ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate,

the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening formed in the insulating layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening having a diameter 1/2 or less of the outer diameter of the connection metal layer,

wherein the input/output signal pin is directly connected

by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[Claim 4] The ceramic wiring substrate according to claim 1, 2, or 3, wherein the connection through hole opening widens as it extends toward the input/output signal pin.

[Claim 5] The ceramic wiring substrate according to claim 1, 2, or 3, wherein the stress relaxation layer is formed from a stress relaxation base layer comprised mainly of copper or aluminum, and a bonding metal layer comprised mainly of chromium or titanium and formed on each of the lower surface and upper surface of the stress relaxation base layer so that the lower surface of the stress relaxation base layer is bonded to the back surface of the ceramic and the upper surface of the stress relaxation base layer is bonded to the insulating layer.

[Claim 6] The ceramic wiring substrate according to claim 1, 2, or 3, wherein the connection metal layer is formed from a solder diffusion preventive layer comprised mainly of at least one member selected from copper, nickel, an alloy of nickel and copper, and an alloy of nickel and tungsten, a bonding metal layer comprised mainly of chromium or titanium and formed on the side of the insulating layer on the solder diffusion preventive layer so that the connection metal layer is bonded to the insulating layer, and an antioxidant metal layer formed on the soldering

connection surface of the solder diffusion preventive layer.

[Claim 7] A ceramic wiring substrate-mounted structure comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

a thin film multilayer wiring circuit connected to the wiring conductor and provided on the front surface of the ceramic wiring substrate, and

a semiconductor integrated circuit connected by soldering to a solder connection terminal formed on the surface of the thin film multilayer wiring circuit,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a circular form adhering to the

surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[Claim 8] A ceramic wiring substrate-mounted structure comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

a thin film multilayer wiring circuit connected to the wiring conductor and provided on the front surface of the ceramic wiring substrate, and

a semiconductor integrated circuit connected by soldering to a solder connection terminal formed on the surface of the thin film multilayer wiring circuit,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter smaller than the root outer diameter of the input/output signal pin, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[Claim 9] A ceramic wiring substrate-mounted structure comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

a thin film multilayer wiring circuit connected to the wiring conductor and provided on the front surface of the ceramic wiring substrate, and

a semiconductor integrated circuit connected by soldering to a solder connection terminal formed on the surface of the thin film multilayer wiring circuit,

wherein the solder connection electrode is formed on the

back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a circular form adhering to the surface of the stress relaxation layer through a connection through hole opening formed in the insulating layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening having a diameter 1/2 or less of the outer diameter of the connection metal layer,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered

with the cover coat layer.

[Claim 10] A ceramic wiring substrate-mounted structure comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin, and

a printed wiring board to which the input/output signal pin is connected,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress

relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[Claim 11] A ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate,

the ceramic wiring substrate comprising a solder connection electrode,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to be subjected to connection by soldering, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer

in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer, is directly subjected to connection by soldering.

[Claim 12] A ceramic wiring substrate-mounted structure

comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode,

a thin film multilayer wiring circuit connected to the wiring conductor and provided on the front surface of the ceramic wiring substrate, and

a semiconductor integrated circuit connected by soldering to a solder connection terminal formed on the surface of the thin film multilayer wiring circuit,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to be subjected to connection by soldering, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress

relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer, is directly subjected to connection by soldering.

[Claim 13] A ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate,

the ceramic wiring substrate comprising a solder connection electrode,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to be subjected to connection by soldering, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer

in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer, is further directly subjected to connection by soldering.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Field of Industrial Utilization]

The present invention relates to a ceramic wiring substrate which is a thick film multilayer ceramic substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, and comprising a connection electrode particularly advantageous to soldering for microelectrode called microsoldering, and a ceramic wiring substrate-mounted structure comprising the same.

[0002]

[Prior Art]

With respect to a module circuit board with high mounting density obtained by mounting an input/output signal pin and others directly on a thick film multilayer ceramic substrate by soldering, the prior art techniques are described in Japanese Unexamined Patent Publication Nos. Sho 63-110697 and Hei 6-53648.

[0003]

The former has a description showing that a circuit interconnection is formed using a zirconium layer as a bonding layer disposed between a ceramic or polyimide structure and a copper or aluminum layer.

[0004]

The latter has a description about a wiring board having formed on a thick film multilayer ceramic substrate a thin film

wiring layer comprising an insulating film comprised of a polymer material and a circuit wiring film, which are alternately stacked, wherein a connection pad for connecting electronic parts is formed in a part of the circuit wiring film in the thin film wiring layer and the outer periphery of the connection pad is covered with an insulating film.

[0005]

[Problem to be Solved by the Invention]

When the connection pad is formed on the thin film wiring layer to mount a semiconductor device as described in the latter in the above prior art techniques, a shearing force exerted on them is absorbed to some extent by the resin layer in the underlying stacked films, which layer is comprised of a material having a relatively high elastic modulus, such as a polyimide resin, to remove an adverse effect on the ceramic substrate, avoiding a danger that the ceramic substrate is broken.

[0006]

However, when an electrode for connection is formed directly on or in the immediate vicinity of the back surface of the ceramic substrate and connected by soldering to, for example, an input/output signal pin as described in the former in the above prior art techniques, a stress strain on the ceramic substrate caused by the entire connection electrode is increased particularly due to a film stress of the stacked films themselves

constituting the connection electrode or a shrinkage stress of the solder itself which is used in a relatively large amount, and further the accumulation of strains caused due to the shape of the connection electrode or the like results in a local stress exceeding the strength of the ceramic substrate to cause a crack in the ceramic substrate, leading to a fatal defect, such as breakage of the ceramic substrate. Specifically, as shown in Fig. 8, on thick film multilayer ceramic substrate (ceramic structure) 1 is formed connection electrode 20 comprising zirconium layer 24 as a bonding layer having a thickness of 30 to 2,000 angstroms, copper, aluminum, or gold layer 23 having a thickness of 2 to 20 μm, solder reaction/diffusion preventive layer 24 having a thickness of 0.5 to 3.0 μm, and gold layer 21 having a thickness of 0.3 to 1.0 μm as an antioxidant layer on the surface, which layers are stacked on one another. When signal pin 3 is connected by soldering to the connection electrode in this state, a film stress of the thin film materials themselves constituting the connection electrode is caused as a shearing force at the end portion, and further a shrinkage stress of the solder, which has wetted and spread the connection electrode surface, is caused at the end of the solder, so that stress concentration occurs at end portion 25 of the joint area with the ceramic substrate to cause a crack in the ceramic substrate

from this site as a starting point, leading to breakage of the ceramic substrate. Thus, in the former in the above prior art techniques, a task to prevent the ceramic substrate from suffering breakage upon connecting by soldering, for example, an input/output signal pin to an electrode for connection, which is formed directly on or in the immediate vicinity of the back surface of the ceramic substrate, has not been considered. Further, in the latter in the above prior art techniques, the task to prevent the ceramic substrate from suffering breakage has also not been considered.

[0007]

An object of the present invention is to solve the above-mentioned problems accompanying the prior art techniques and to provide a ceramic wiring substrate which is advantageous in that a solder connection electrode having high reliability such that it causes no breakage of the thick film multilayer ceramic substrate can be formed directly on or in the immediate vicinity of the back surface of the thick film multilayer ceramic substrate, and a ceramic wiring substrate-mounted structure comprising the same.

[0008]

[Means to Solve the Problem]

For attaining the above object, the present invention is directed to a ceramic wiring substrate having as an internal

layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin, wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer or a diameter smaller than the root outer diameter of the input/output signal pin, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer,

and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[0009]

Further, the present invention is directed to a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin, wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening formed in the insulating layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening having a diameter 1/2 or less of the outer diameter of the connection metal layer,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[0010]

Furthermore, the present invention is the ceramic wiring substrate, wherein the connection through hole opening widens as it extends toward the input/output signal pin. Further, the present invention is the ceramic wiring substrate, wherein the stress relaxation layer is formed from a stress relaxation base layer comprised mainly of copper or aluminum, and a bonding metal

layer comprised mainly of chromium or titanium and formed on each of the lower surface and upper surface of the stress relaxation base layer so that the lower surface of the stress relaxation base layer is bonded to the back surface of the ceramic and the upper surface of the stress relaxation base layer is bonded to the insulating layer. Further, the present invention is the ceramic wiring substrate, wherein the connection metal layer is formed from a solder diffusion preventive layer comprised mainly of at least one member selected from copper, nickel, an alloy of nickel and copper, and an alloy of nickel and tungsten, a bonding metal layer comprised mainly of chromium or titanium and formed on the side of the insulating layer on the solder diffusion preventive layer so that the connection metal layer is bonded to the insulating layer, and an antioxidant metal layer formed on the soldering connection surface of the solder diffusion preventive layer.

[0011]

Further, the present invention is directed to a ceramic wiring substrate-mounted structure comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

a thin film multilayer wiring circuit connected to the wiring conductor and provided on the front surface of the ceramic wiring substrate, and

a semiconductor integrated circuit connected by soldering to a solder connection terminal formed on the surface of the thin film multilayer wiring circuit,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer or a diameter smaller than the root outer diameter of the input/output signal pin, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer.

[0012]

Further, the present invention is directed to a ceramic wiring substrate-mounted structure comprising:

a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode and an input/output signal pin,

a thin film multilayer wiring circuit connected to the wiring conductor and provided on the front surface of the ceramic wiring substrate, and

a semiconductor integrated circuit connected by soldering to a solder connection terminal formed on the surface of the thin film multilayer wiring circuit,

wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to which the input/output signal pin is connected, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a circular form adhering to the surface of the stress relaxation layer through a connection through hole opening formed in the insulating layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer; and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening having a diameter 1/2 or less of the outer diameter of the connection metal layer,

wherein the input/output signal pin is directly connected by soldering to the surface of the connection metal layer in

the solder connection electrode, which surface is not covered with the cover coat layer.

[0013]

Furthermore, the present invention is directed to a ceramic wiring substrate having as an internal layer a wiring conductor led to the back surface and front surface of the ceramic wiring substrate, the ceramic wiring substrate comprising a solder connection electrode, wherein the solder connection electrode is formed on the back surface side of the ceramic wiring substrate to be subjected to connection by soldering, and comprises:

a stress relaxation layer connected directly to the wiring conductor, the stress relaxation layer comprising a metal layer in a substantially circular form adhering to the back surface of the ceramic;

an insulating layer covering the back surface of the ceramic including the surface of the stress relaxation layer, and being comprised of an organic material;

a connection metal layer in a substantially circular form adhering to the surface of the stress relaxation layer through a connection through hole opening, formed in the insulating layer, having a diameter 1/2 or less of the outer diameter of the stress relaxation layer, and covering the surface of the insulating layer so that the outer diameter of the connection metal layer is smaller than the outer diameter of the stress relaxation layer;

and

a cover coat layer covering the surface outer periphery and side of the connection metal layer and the insulating layer, and being comprised of an organic material,

wherein the stress directly applied to the stress relaxation layer from the connection metal layer is relaxed by the connection through hole opening,

wherein the surface of the connection metal layer in the solder connection electrode, which surface is not covered with the cover coat layer, is further directly subjected to connection by soldering.

[0014]

[Operation]

By the way, when a metal film including a thin film as a representative example is formed on ceramic substrate 1, the film stress of the film itself causes a stress in ceramic substrate 1. Also, when a pattern, such as a solder connection electrode, is formed, a stress is concentrated on the pattern form. The occurrence of stress concentration in ceramic substrate 1 due to stacking of metal films is shown in Fig. 6. Fig. 6(a) shows a case where, on ceramic substrate 1, for example, Cu (thickness: about 4 μm) in a predetermined pattern is formed as stress relaxation layer 34. Fig. 6(b) shows a case where similarly, on ceramic substrate 1, for example, an Ni-W alloy (thickness:

about 2 μm) in a predetermined pattern having, for instance, radius R2 smaller by ΔR than radius R4 of stress relaxation layer 34 is formed as connection metal layer 32. Fig. 6(c) shows a case where the both thin films are stacked and formed in a predetermined pattern. Stress strains caused in the plane of ceramic substrate 1 under the above conditions were analyzed using the values for physical properties of the constituent materials, and the results are shown in characteristics diagrams of Figs. 6(d) and 6(e). Fig. 6(d) shows the both stresses of the individual thin films, which indicates that the value of stress 61 caused by connection metal layer 32 is larger than that of stress 62 caused by stress relaxation layer 34. However, even when these layers are stacked under conditions such that, for instance, radius R2 of connection metal layer 32 is smaller by ΔR than radius R4 of stress relaxation layer 34, the strain caused at the edge face of connection metal layer 32 is relaxed by the effect of the underlying stress relaxation layer 34, but the stacked films collectively suffer a large strain caused at the edge face of stress relaxation layer 34 as indicated by stress 63 in Fig. 6(e). When soldering 36 is further conducted in this state as shown in Fig. 7(a), for instance, cover coat layer 35 for suppressing the area wetted with the solder is formed to separate the outer periphery of connection metal layer 32 from

the outer periphery of the solder, making it possible to avoid the accumulation of strains. However, as shown in Fig. 7(b), without being affected by cover coat layer 35, stress 64 of the solder is added particularly to the edge face of connection metal layer 32 and, as a result, stress 64 applied to connection metal layer 32 propagates directly to stress relaxation layer 34 which had adhered to the outer periphery of connection metal layer 32, so that the concentrated stress equal to or larger than strength δ_0 of ceramic substrate 1 is applied to the outer periphery of stress relaxation layer 34 to cause a crack in ceramic substrate 1, leading to breakage of the ceramic substrate.

[0015]

The present invention has been made based on the above results of analysis. Specifically, in the present invention, by virtue of the above-described construction, even when a solder connection electrode for connecting by soldering, e.g., an input/output signal pin is formed directly on the back surface of the thick film multilayer ceramic substrate, the stress strain is dispersed in the connection metal layer by a connection through hole opening having diameter ϕD_1 which is 1/2 or less of outer diameter ϕD_4 of the stress relaxation layer, 1/2 or less of outer diameter ϕD_2 of the connection metal layer, or smaller than root outer diameter ϕD_0 of the input/output signal pin, an insulating

layer comprised of an organic material sandwiched between the connection metal layer and the stress relaxation layer, and a cover coat layer covering the surface outer periphery of the connection metal layer, and the connection metal layer and stress relaxation layer adhere to each other and are joined together in the connection through hole opening having limited diameter ϕD_1, and therefore the stress strain is prevented from propagating directly to the stress relaxation layer to suppress stress concentration on the ceramic substrate at the outer periphery of the stress relaxation layer, making it possible to prevent the formation of a crack in the ceramic substrate, namely, the occurrence of a fatal defect, such as breakage of the ceramic substrate, thus realizing connection by soldering with high reliability of, e.g., an input/output signal pin to the solder connection electrode formed on the back surface of the thick film multilayer ceramic substrate. From the state of the soldering shown in Fig. 3, taking into consideration the fact that the outer periphery of connection metal layer 2 at L_1 = about 0.1 mm is covered with cover coat layer 5, root outer diameter ϕD_0 of input/output signal pin 3 is about 1/2 of outer diameter ϕD_2 of connection metal layer 2, and it is apparent that diameter ϕD_1 of the connection through hole opening is preferably equal to or smaller than root outer diameter ϕD_0 of signal pin 3 or

1/2 or less of outer diameter ϕD_2 of connection metal layer 2. In Fig. 3, a case is shown in which difference L_2 between radius $\phi D_2/2$ of connection metal layer 2 and radius $\phi D_4/2$ of the stress relaxation layer is about 0.2 mm, but, it is apparent that, when connection metal layer 2 is formed so that this difference is reduced, diameter ϕD_1 of the connection through hole opening is preferably 1/2 or less of outer diameter ϕD_4 of the stress relaxation layer.

[0016]

Further, from the stress characteristics shown in Fig. 3, diameter ϕD_1 of the connection through hole opening is most desirably 2/3 or less of root outer diameter ϕD_0 of input/output signal pin 3. It is noted that, when diameter ϕD_1 of the connection through hole opening is reduced, the resistance of connection between connection metal layer 3 and stress relaxation layer 4 is increased, and therefore, diameter ϕD_1 of the connection through hole opening is desirably 40 μm or more.

[0017]

That is, in the present invention, by virtue of the above-described construction, a cover coat layer is formed on the surface outer periphery of the connection metal layer and therefore, the outer periphery of the solder and the outer periphery of the connection metal layer are not placed on one

another, and further a through hole opening having a diameter, which is 1/2 of the outer diameter of the stress relaxation layer, 1/2 of the outer diameter of the connection metal layer, or even smaller than the root outer diameter of signal pin 3 to be connected, is formed in the interlayer dielectric film to separate and disperse the originating points of stress strain, so that the stress strain is prevented from propagating directly to the stress relaxation layer, confirming that characteristics having a satisfactory margin for the strength of the ceramic substrate are obtained.

[0018]

Particularly, in the circuit-mounted module substrate for computer of the present invention and others, which require an operation (repair) of replacing a part, such as a signal pin connected and mounted onto the substrate, the solder in the joint is melted every operation and the diffusion reaction of solder proceeds and therefore, according to the frequency of repair, the thickness of the diffusion preventive layer metal in the connection metal layer must be larger than usual. Even in such a case, by the present invention, connection by soldering with high reliability of, e.g., an input/output signal pin can be realized without causing breakage of the ceramic substrate.

[0019]

[Embodiments]

The embodiment of the present invention will be described in detail with reference to the drawings.

[0020]

First, the ceramic wiring substrate-mounted structure comprising the ceramic wiring substrate of the present invention is described based on the embodiment shown in Fig. 4. Specifically, Fig. 4 is a cross-sectional view of the main structure of the ceramic wiring substrate-mounted structure comprising the ceramic wiring substrate. Thick film multilayer ceramic substrate 1 has internal layer wiring conductor 11 which is led to the back surface as indicated by 7 and which is also led to the front surface, and is formed from, for example, alumina, mullite, or glass ceramic. Thick film multilayer ceramic substrate 1 has formed thereon thin film multilayer wiring circuit 10 having a thin film multilayer structure in which a wiring to be connected to wiring conductor 11 led to the front surface and an interlayer dielectric film of an organic material, such as a polyimide resin, are stacked on one another. Solder connection terminal 12 is formed on the surface of thin film multilayer wiring circuit 10, and solder connection terminal 12 is connected and mounted onto connection terminal 15 of semiconductor integrated circuit (LSI) 14 by solder 13.

[0021]

On the back surface of thick film multilayer ceramic

substrate 1, solder connection electrode 18 for connecting wiring conductor 7 led to the back surface and input/output signal pin 3 is provided. A number of input/output signal pins 3 provided on the back surface of thick film multilayer ceramic substrate 1 are inserted into and connected to printed wiring board 16 having formed wiring pattern 17 or connectors. Input/output signal pins 3 are subjected to soldering if necessary after being inserted into printed wiring board 16. The ceramic wiring substrate-mounted structure comprising the ceramic wiring substrate of the present invention has the construction described above. An example of solder connection electrode 18 provided on the back surface of thick film multilayer ceramic substrate 1 in the present invention is described below with reference to Figs. 1 and 2.

[0022]

First, stress relaxation metal layer 4 adheres to and is joined to the back surface of thick film multilayer ceramic substrate 1 formed from, for example, glass ceramic, wherein stress relaxation metal layer 4 is in a circular form (that may be a quadrangular form having arch-form corners, which approximates to a circular form) having outer diameter ϕD_4 of 1.2 to 2.0 mm (in Fig. 3, about 1.6 mm), and comprises bonding layer 4b of Cr or Ti (thickness: 0.05 to 0.2 μm), stress relaxation

metal layer base 4a of Cu or Al (thickness: 4 to 6 μm), and bonding layer 4c of Cr or Ti (thickness: 0.03 to 0.1 μm). That is, stress relaxation metal layer 4 adheres to and is joined to the back surface of thick film multilayer ceramic substrate 1 through bonding layer 4b, and further adheres to wiring conductor 7 having a diameter of 50 to 100 μm buried in thick film multilayer ceramic substrate 1, achieving electrical connection.

[0023]

The surface of stress relaxation metal layer 4 is covered with interlayer dielectric layer 6 (thickness: 4 to 10 μm) comprised of an organic material, such as a polyimide resin, and through hole opening 9 having diameter ϕD_1 of 50 to 400 μm is formed so that the surface of stress relaxation metal layer 6 is exposed. In Fig. 3, a case is shown in which diameter ϕD_1 of through hole opening 9 is 240 μm. Through hole opening 9 has inclination such that the opening widens as it extends toward signal pin 3.

[0024]

With respect to the surface of interlayer dielectric layer 6 and through hole opening 9, solder connection metal layer 2, which is in a circular form (that may be a quadrangular form having arch-form corners, which approximates to a circular form) having outer diameter ϕD_2 of 1.0 to 1.4 mm (in Fig. 3, about 1.2

mm), and which comprises bonding layer 2b of Cr or Ti (thickness: 0.03 to 0.1 μm) and connection metal layer base 2a of Cu, Ni, an Ni-Cu alloy, or an Ni-W alloy (thickness: 1.5 to 3 μm), adheres to and is joined to the surface of stress relaxation metal layer 4 in through hole opening 9, and adheres to the surface of interlayer dielectric layer 6. That is, solder connection metal layer 2 adheres to and is joined to the surface of stress relaxation metal layer 4 only in through hole opening 9. As mentioned above, interlayer dielectric layer 6 is comprised of an organic material, such as a polyimide resin, and therefore stress strain caused on solder connection metal layer 2 is dispersed in solder connection metal layer 2 and propagates to stress relaxation metal layer 2 only through through hole opening 9 having ϕD_1 of 50 to 400 μm, so that the stress strain is considerably reduced.

[0025]

The surface of interlayer dielectric layer 6 is covered with cover coat layer 5 (thickness: 3 to 7 μm) comprised of an organic polyimide resin film so that the outer periphery of solder connection metal layer 2 at L_1 = 50 to 200 μm is covered.

[0026]

Au Plating film (thickness: about 0.05 μm) 28 is formed as an antioxidant layer on the surface of solder connection metal layer 2 in an opening portion (solder wetting region) which is

not covered with cover coat layer 5. Au Plating film 28 is connected by soldering to input/output signal pin 3 having a root outer diameter: ϕD_0 = ϕ 0.4 to 0.8 mm (in Fig. 3, about 0.6 mm) (material: Cu alloy) using, for example, a solder material: Au-20 wt% Sn (melting point = 280°C).

[0027]

Next, the distribution of stress (Kgf/mm^2) exerted on the back surface of thick film multilayer ceramic substrate 1 is described with reference to Fig. 3, in connection with the structure of the solder connection electrode in the present invention. As indicated by solid line 19 in Fig. 3, differing from the stress indicated by solid line 65 in Fig. 7, the stress at the outer periphery of stress relaxation metal layer 4 does not exceed strength δ_0 which breaks ceramic substrate 1. Specifically, as apparent from solid line 19, interlayer dielectric layer 6 is comprised of an organic material, such as a polyimide resin, and therefore stress strain caused on solder connection metal layer 2 is dispersed in solder connection metal layer 2 and propagates to stress relaxation metal layer 2 only through through hole opening 9 having ϕD_1 of 50 to 400 μm, and, as a result, the stress concentrated places are dispersed and the stress can be dramatically reduced so that a margin for strength δ_0 which breaks ceramic substrate 1 is obtained to prevent the

formation of a crack in ceramic substrate 1, thus making it possible to form a solder connection electrode with high reliability for connecting by soldering signal pin 3 or the like directly on or in the immediate vicinity of the back surface of ceramic substrate 1. Thus, a ceramic wiring substrate-mounted structure obtained using the above ceramic wiring substrate has high reliability such that it suffers no breakage of ceramic substrate 1.

[0028]

Further, when the diameter of through hole opening 9 is even smaller than root diameter ϕD_0 of signal pin 3 or even smaller than 1/2 of outer diameter ϕD_2 of solder connection metal layer 2, there can be obtained a more satisfactory margin for strength δ_0 which breaks ceramic substrate 1. Specifically, in a region inside of root diameter ϕD_0 of signal pin 3, the direction of the stress exhibits tendency of shrinkage. This is because the thermal expansion coefficient (α) of signal pin 3 and the solder material is larger than the thermal expansion coefficient of ceramic substrate 1, and therefore a portion which is not affected by the stress concentration due to, e.g., a change of shape becomes a field of stress in shrinkage. By virtue of this phenomenon, when the through hole opening diameter (ϕD_1) in interlayer dielectric film 6 is smaller than the root diameter (ϕD_0) of signal

pin 3 or smaller than 1/2 of outer diameter ϕD_2 of solder connection metal layer 2, the stress concentration accumulated around the outer periphery of solder connection metal layer 2 shifts to a region on the shrinkage side near the end portion of the diameter (ϕD_1) of through hole opening 9 in interlayer dielectric film 6, so that the stress concentration can be reduced and its effect is negligible. Further, by forming cover coat layer 5, L_1 is formed between the outer periphery of solder connection metal layer 2 and the outer periphery of the solder wetting to make it possible to separate the accumulation, so that the stress strain points exerted on ceramic substrate 1 can be more surely dispersed, thus realizing solder connection having a satisfactory margin for strength δ_0 of ceramic substrate 1 directly on or in the immediate vicinity of ceramic substrate 1.

[0029]

Next, a method for producing the ceramic wiring substrate of the present invention is described in accordance with the steps shown in Fig. 5. Thick film multilayer ceramic substrate 1 is produced in a. thick film circuit substrate step. Specifically, the thick film multilayer ceramic substrate can be produced by printing internal conductor wiring 11 on a high resistance material, such as alumina, mullite, or glass ceramic, by a method, such as screen printing, to prepare a green sheet,

and stacking the green sheets and subjecting the stacked sheet to sintering.

[0030]

Next, in steps b through f, on the back surface of thick film multilayer ceramic substrate 1, solder connection electrode 18 for connecting by soldering signal pin 3 or the like is produced.

[0031]

First, in b. matching layer (stress relaxation metal layer) pattern formation step, on the back surface of thick film multilayer ceramic substrate 1, which surface has been abraded and smoothed with high fineness, stress relaxation metal layer 4 serving as stress relaxation for solder connection metal layer 2 is formed as follows. Thin films of Cr or Ti/Cu or Al/Cr or Ti are formed by sputtering in this order from the bottom, and patterned into a substantially circular form by etching, so that the resultant layer is connected to wiring conductor 7 and directly adheres to thick film multilayer ceramic substrate 1. The respective thin films have thicknesses of about 0.1 μm/about 5 μm/about 0.05 μm. In this instance, in the etching for Cr, a potassium ferricyanide/potassium hydroxide mixture is used, and, in the etching for Cu, a phosphoric acid/nitric acid mixture is used.

[0032]

Next, in c. interlayer dielectric layer formation step, a polyimide resin is formed on the back surface of thick film multilayer ceramic substrate 1 by a spin coating method, and subjected to heat treatment at 350°C to form interlayer dielectric layer 6. The formed film has a thickness of about 6 μm. Then, through hole opening 9 is processed in the resultant polyimide film by a method in which a desired resist pattern is formed on the surface of interlayer dielectric layer 6, followed by etching using a hydrazine/ethylenediamine mixture, or a convenient method in accordance with a conventional photolithography technique using a polyimide resin itself having a function of photosensitivity.

[0033]

Next, in d. solder connection metal layer formation step, Cr or Ti/Cu, Cu, Ni, Ni-Cu alloy, or Ni-W alloy films are formed as solder connection metal layer 2 on the above-obtained layer by the same method as that for stress relaxation metal layer 4, i.e., by sputtering and etching. The resultant films have thicknesses of about 0.05 μm/2 μm. In this instance, in the etching for the Ni-W alloy film, a hydrofluoric acid etchant is used. Next, in e. cover coat layer formation step, cover coat layer 5 is formed on the surface by the same method as that for interlayer dielectric layer 6. The resultant film has a thickness

of about 4 μm. Subsequently, in f. plating film formation step, for the purposes of improving the solder wettability and preventing oxidation, an Au plating film is formed in the solder connection region formed as opening in cover coat layer 5 so that the resultant film has a thickness of about 0.05 μm. As shown in Figs. 1 and 2, input/output signal pin 3 was connected by soldering to solder connection electrode 18 produced in the above steps on thick film multilayer ceramic substrate 1. The solder material used is Au-20 wt% Sn (melting point = 280°C).

[0034]

With respect to the construction produced and connected in the above-described steps, the results of analysis of the stress strain caused in thick film multilayer ceramic substrate 1 by the whole of solder connection electrode 18 show that, as mentioned above, for avoiding accumulation of the strains concentrated on the end portions of the individual constituent films, gaps L_1, L_2 individually between the outer periphery of the pattern opening which is not covered with surface cover coat layer 5, the outer periphery of solder connection metal layer 2, and the outer periphery of stress relaxation metal layer 4 are rendered 0.05 mm or more so that the strain concentration is dispersed. Further, when the through hole opening diameter (ϕD_1) in interlayer dielectric layer 6 is even smaller than top diameter (ϕD_0) of

input/output signal pin 3 to be connected, the collective stress strain caused in thick film multilayer ceramic substrate 1 has characteristics such that the local concentration is dispersed, so that solder connection of a signal pin or the like having a satisfactory margin for strength δ_0 of thick film multilayer ceramic substrate 1 and having high reliability can be achieved directly on or in the immediate vicinity of thick film multilayer ceramic substrate 1, making it possible to remove a fatal defect factor, such as breakage of the ceramic substrate.

[0035]

Based on the above results of analysis, the present inventors have subsequently conducted a tensile test in which, using the ceramic wiring substrate having an input/output signal pin connected to the solder connection electrode in the present invention, the signal pin is forcibly peeled off. As a result, all the substrates showed a mode such that the signal pin itself was broken and suffered no breakage of the ceramic substrate, which indicates that connection having ideal high reliability in respect of the solder connection electrode has been achieved.

[0036]

[Effect of the Invention]

By the present invention, in the solder connection electrode provided directly on or in the immediate vicinity of the ceramic wiring substrate, by inserting an interlayer dielectric film

between the stress relaxation metal layer and the solder connection metal layer, the stress can be further relaxed. Further, when the gaps between the outer peripheries of the pattern forms in the cover coat layer formed on the surface and the both metal layers are separated, or when the diameter of the through hole opening in the interlayer dielectric film is 1/2 or less of the outer diameter of the stress relaxation metal layer, 1/2 or less of the outer diameter of the solder connection metal layer, or smaller than the root outer diameter of the signal pin to be connected, the accumulation of strains caused by the stresses of the individual constituents can be avoided, so that the solder connection electrode is improved in mechanical strength for the ceramic substrate to make it possible to remove a defect factor, such as breakage of the ceramic substrate, thus achieving an effect such that not only the ceramic wiring substrate but also the ceramic wiring substrate-mounted structure are remarkably improved in reliability.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1] Fig. 1 is a cross-sectional view showing one example of a solder connection electrode provided on the back surface of the thick film multilayer ceramic substrate of the present invention.

[Fig. 2] Fig. 2(a) is a cross-sectional view in elevation, and Fig. 2(b) is a plan view, each of which shows one example

of a solder connection electrode provided on the back surface of the thick film multilayer ceramic substrate of the present invention.

[Fig. 3] Fig. 3 is a cross-sectional view showing one example of a solder connection electrode for connecting by soldering an input/output signal pin, which electrode is provided on the back surface of the thick film multilayer ceramic substrate of the present invention, and a diagram showing the characteristics of stress distribution caused in the thick film multilayer ceramic substrate upon connecting by soldering the input/output signal pin.

[Fig. 4] Fig. 4 is a cross-sectional view of the main structure of the ceramic wiring substrate-mounted structure (thick film-thin film hybrid module substrate) of the present invention.

[Fig. 5] Fig. 5 is a diagram showing the process for producing a solder connection electrode provided on the back surface of the thick film multilayer ceramic substrate of the present invention.

[Fig. 6] Fig. 6 is a diagrammatic view illustratively showing the characteristics of stresses caused when metallic thin films are formed and stacked on the thick film multilayer ceramic substrate.

[Fig. 7] Fig. 7 is a diagrammatic view illustratively

showing the characteristics of a stress caused when metallic thin films are stacked on the thick film multilayer ceramic substrate and further subjected to soldering.

[Fig. 8] Fig. 8 is a cross-sectional view showing a solder connection electrode in the prior art, which is provided on the back surface of a thick film multilayer ceramic substrate and used for connecting an input/output signal pin by soldering.

[Description of the Reference Numerals]

1: Thick film multilayer ceramic substrate (Ceramic wiring substrate)

2: Solder connection metal layer

3: Signal pin

4: Stress relaxation metal layer

5: Cover coat layer

6: Interlayer dielectric layer

7; 11: Wiring conductor

8; 13: Solder

9: Through hole opening

10: Thin film multilayer wiring circuit

12: Connection terminal

14: Semiconductor integrated circuit (LSI)

16: Printed wiring board

18: Solder connection electrode